



(11) Publication number:

0 560 228 A1

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 93103578.6

(61) Int. Cl. 5: H03D 7/12

(22) Date of filing: 05.03.93

(30) Priority: 11.03.92 JP 52425/92

(43) Date of publication of application:
15.09.93 Bulletin 93/37

(84) Designated Contracting States:
DE FR GB NL SE

(71) Applicant: SUMITOMO ELECTRIC INDUSTRIES,
LIMITED
5-33, Kitahama 4-chome Chuo-ku
Osaka(JP)

(72) Inventor: Shiga, Nobuo, c/o Yokohama Works
of Sumitomo
Electric Industries, Ltd., 1, Taya-cho,
Sakae-ku
Yokohama-shi, Kanagawa(JP)

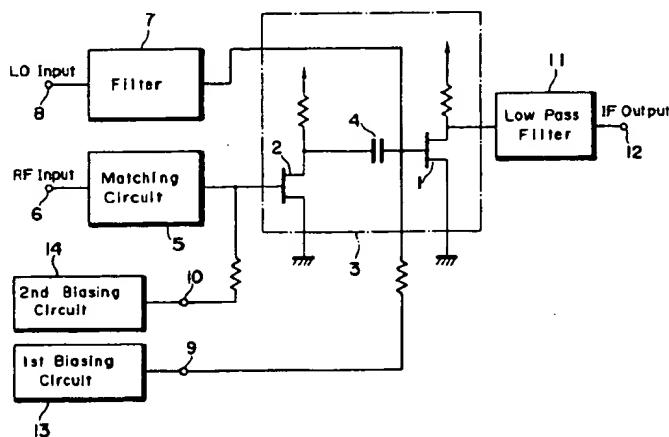
(74) Representative: Kahler, Kurt, Dipl.-Ing.
Patentanwälte Kahler, Käck & Fiener
Maximilianstrasse 57 Postfach 12 49
D-87712 Mindelheim (DE)

(54) Mixer circuit.

(57) An FET mixer circuit having a stable input impedance uses two tandem-connected GaAs MESFET's (1, 2) of pulse doped structure instead of a conventional MESFET or a HEMT, as an active device. A gate biasing point for the FET (1) is set around a pinch-off point of a mutual conductance, and a gate biasing point for the FET (2) is set in a

region which assures non-change of a mutual conductance with respect to the increase of a gate voltage. Thus, a mixer circuit having a good isolation characteristic for an RF signal and a local oscillation signal and exhibiting substantially no change in the input impedance is attained.

Fig. 1



EP 0 560 228 A1

BACKGROUND OF THE INVENTIONField of the Invention

The present invention relates to a mixer circuit to be used for a frequency converter circuit or a measuring instrument.

Related Background Art

As an information network system has recently developed rapidly, a demand for a satellite communication system has also rapidly increased and a frequency band thereof is shifting toward a high frequency region. In such a satellite communication system, a down-converter for converting a high frequency signal to a low frequency signal is required, and a demand for a mixer circuit used therefor is also increasing. A conventional mixer circuit uses a diode, a bipolar transistor or a field effect transistor (FET) as an active device. As the FET, a conventional Schottkey gate FET (MESFET) or a high electron mobility transistor (HEMT) is usually used.

A biggest problem is designing the mixer circuit using the FET or the FET mixer circuit is that a gate voltage of the FET significantly swings because a local oscillation signal is a large amplitude signal. The change in the gate voltage causes a change in a mutual conductance g_m of the FET, which in turn causes a change in a gate-source capacitance C_{gs} or an input impedance. When viewed from an RF signal input terminal, the FET mixer circuit operates with a large change in an input impedance of the circuit as a function of a time corresponding to the swing of the local oscillation signal. As a result, the design is hard to attain and a stable operation is not expected.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a mixer circuit in which an input impedance does not change and which operates stably.

In order to achieve the above object, the mixer circuit of the present invention comprises first and second FET's, and a gate electrode of the second FET is connected to an RF signal input terminal, a gate electrode of the first FET is connected to a local oscillation signal input terminal and a drain of the second FET, and a drain of the first FET is connected to an IF (intermediate frequency) signal output terminal. The first and second FET's are MESFET's of pulse doped structure.

In accordance with the mixer circuit of the present invention, the input impedance of the circuit viewed from the RF signal input terminal is not affected because the local oscillation signal is not

applied to the gate of the second FET to which the RF signal is applied. Further, where a gate biasing point of the second FET is set in a flat region of the mutual conductance by utilizing a characteristic inherent to the MESFET of the pulse doped structure, that is, "it has the flat region in which the mutual conductance does not change with the gate voltage", a change of the input impedance due to the RF signal itself does not occur. By making a gate width of the second FET shorter than that of the first FET arranged at the output, a power consumption can be reduced compared to a conventional circuit in which a single FET is used and the RF signal and the local oscillation signal are applied to the gate thereof and the IF signal is taken out of the drain thereof. Further, since the RF signal and the local oscillation signal are applied to the different FET's, an isolation characteristic between the FET's is superior to that attained when the active device comprises a single FET.

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not to be considered as limiting the present invention.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram of a mixer circuit in accordance with one embodiment of the present invention,

Fig. 2 shows a sectional view of a GaAs MESFET of pulse doped structure, and

Fig. 3 shows a graph of gate voltage V_g Vs mutual conductance g_m of the GaAs MESFET of the pulse doped structure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1, two GaAs MESFETs 1 and 2 of pulse doped structure connected in tandem are used as an active device 3 of the mixer circuit. Fig. 2 shows a sectional view of a structure of the GaAs MESFET 1 or 2 of the pulse doped structure. An undoped p- GaAs buffer layer 22, an Si-doped pulse doped GaAs layer 23 which serves as an

activation layer, and an undoped n- GaAs cap layer 24 are sequentially laminated on a semi-insulative GaAs substrate 21 by an epitaxial growth method, and n+ ion implantation regions 28 and 29 which extend from a surface to a top of the buffer layer 22 are formed in a source region and a drain region. A gate electrode 25 which makes a Schottkey contact with the cap layer 24 is formed in a region on the cap layer 24 which is sandwiched by the source region and the drain region, and a source electrode 26 and a drain electrode 27 which make ohmic contacts with the cap layer 24, respectively, are formed in the source region and the drain region. A gate length is 0.5 μm . An example of the thickness is that the buffer layer 22 is 10,000 Angstrom, the pulse doped layer 23 is 100 Angstrom, and the cap layer 24 is 300 Angstrom. An impurity concentration of the pulse doped layer 23 is $4.0 \times 10^{18} \text{ cm}^{-3}$. An organic metal vapor phase epitaxial growth (OMVPE) method is used as an epitaxial growth method. Specifically, a Cr-doped GaAs substrate is used and the vapor phase growth is carried out by introducing TMG (trimethyl gallium) and AsH₃ as source gas and SiH₄ as dopant at a pressure of 60 Torr and a temperature of 650 °C. A source gas introduction V/III ratio is 6 for the buffer layer 22, 40 for the pulse doped layer 23 and 100 for the cap layer 24. The MESFET's 1 and 2 of the pulse doped structure have different gate widths. The gate width of the FET 1 is approximately 300 μm and the gate width of the FET 2 is approximately 50 - 100 μm .

An input terminal 6 of the RF (radio frequency) signal is connected to the gate of the MESFET 2 of the pulse doped structure through a matching circuit 5 for matching an input impedance. The drain of the FET 2 is connected to the gate of the FET 1 through a coupling capacitor 4 which couples AC circuits having different DC levels. Thus, an AC component of the signal outputted from the drain of the FET 2 is applied to the gate of the FET 1. An input terminal 8 of the local oscillation (LO) signal is connected to the gate of the FET 1 through a filter 7. As a result, the RF signal applied to the FET 1 through the FET 2 is combined with the LO signal and converted to a lower frequency (an intermediate frequency (IF)) signal.

An output terminal 12 is connected to the drain of the FET 1 through a low pass filter 11 which passes only the intermediate frequency (IF) signal which is the output signal. As a result, the IF signal which is a mixed-down signal of the RF signal is outputted from the output terminal 12. The filter 7 serves to prevent the IF signal generated by the mixer circuit from leaking to the local oscillation circuit connected to the terminal 8. The terminals 9 and 10 are input terminals for applying DC gate bias voltages to the FET 1 and the FET 2, respec-

tively.

An output terminal of a first biasing circuit 13 which supplies a gate bias voltage around a pinch-off voltage to the gate electrode of the FET 1 is connected to the terminal 9. An output terminal of a second biasing circuit 14 which supplies a gate bias voltage to the gate electrode of the FET 2 and whose mutual conductance g_m does not change with the gate voltage is connected to the terminal 10.

The significance of the magnitudes of the bias voltages supplied by the first and second biasing circuits 13 and 14 is explained below.

The mixer circuit of the present embodiment converts the frequency by utilizing the non-linearity of the mutual conductance as the prior art FET mixer circuit does. Accordingly, it is necessary for the FET 1 which carries out the mixing to operate at a gate biasing point which assures that the mutual conductance g_m is non-linear to the gate voltage V_g. On the other hand, it is necessary for the FET 2 for which the stable input impedance is required to operate at a gate biasing point which assures that the mutual conductance g_m is constant with respect to the gate voltage V_g.

Fig. 3 shows a gate voltage V_g Vs mutual conductance g_m characteristic of the GaAs MESFET's 1 and 2 of the pulse doped structure. Four points shown by numerals 32 - 35 may be candidates for the gate biasing point which assures the non-linear mutual conductance g_m to the gate voltage V_g. Namely, a large conversion efficiency may be attained around those points. On the other hand, a flat region 31 is a candidate for the gate biasing point which assures that the input impedance does not significantly change with respect to the swing of the gate voltage. The flat region 31 in which the mutual conductance g_m does not change with the gate voltage V_g is a characteristic which is inherent to the MESFET of the pulse doped structure and not found in the prior art device. The non-change of the mutual conductance g_m means a small change in the input capacitance or the gate-source capacitance C_{gs}, and the input impedance of the FET greatly depends on the gate-source capacitance C_{gs}. Accordingly, so long as the gate voltage V_g changes in the flat region 31, there is no significant change in the input impedance. The input impedance is generally expressed by the following formula, which indicates the great dependency of the input impedance to the gate-source capacitance C_{gs}.

$$Z_{in} = R_g + 1/j\omega C_{gs} + R_{in} + R_s$$

where R_g is a gate resistance, R_{in} is a channel resistance, and R_s is a source resistance.

From the above consideration, the gate biasing point for the FET 1 is to be set around one of the four points 32 - 35, and it is preferable to set the gate biasing point around the point 32, that is, around the pinch-off point in order to minimize the power consumption. For the FET 2, it is preferable to set the gate biasing point in the flat region 31 in which the input impedance is stable with respect to the change in the gate voltage. It is also preferable to minimize the power consumption of the FET 2 like the FET 1. In consideration of the above, it is desirable to set the gate biasing point around the point 33 which is the lowest gate voltage point in the flat region 31.

In the mixer circuit of the present embodiment, the tandem connection of the first GaAs MESFET of the pulse doped structure and the second GaAs MESFET of the pulse doped structure having a shorter gate width than that of the first FET is used as the active device, the gate biasing point of the first FET is set around the pinch-off point of the mutual conductance, and the gate biasing point of the second FET is set in the region in which the mutual conductance does not change with the increase of the gate voltage. Accordingly, the isolation characteristic between the RF signal and the local oscillation signal is good, the input impedance does not substantially change and the power consumption is low.

From the invention thus described, it will be obvious that the invention may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A mixer circuit using FET's as an active device wherein:

 said active device comprises first and second FET's (1, 2),

 a gate electrode of said second FET (2) is connected to an RF signal input terminal (6),

 a gate electrode of said first FET (1) is connected to a local oscillation signal input terminal (8) and a drain of said second FET (2),

 a drain of said first FET (1) is connected to an IF signal output terminal (12), and

 said first and second FET's (1, 2) are MESFET's of pulse doped structure.

2. A mixer circuit according to Claim 1

 wherein said first and second FET's (1, 2) are GaAs MESFET of pulse doped structure.

3. A mixer circuit according to Claim 1 or 2 comprising:

 first biasing means (13) for supplying a gate biasing voltage around a pinch-off voltage to the gate of said first FET (1); and

 second biasing means (14) for supplying a gate biasing voltage assuring non-change of a mutual conductance with respect to a change in a gate voltage.

4. A mixer circuit according to any of Claims 1 to 3

 wherein a gate width of said second FET (2) is shorter than that of said first FET (1).

5. A mixer circuit according to any of Claims 1 to 4

 wherein an impedance matching circuit (5) is provided between the gate electrode of said second FET (2) and the RF signal input terminal (6).

6. A mixer circuit according to any of Claims 1 to 5

 wherein a coupling capacitor (4) is provided between the drain electrode of said second FET (2) and the gate electrode of said first FET (1).

7. A mixer circuit according to any of Claims 1 to 6

 wherein a low pass filter (11) is provided between the drain electrode of said first FET (1) and the IF signal output terminal (12).

8. A mixer circuit according to any of Claims 1 to 7

 wherein a filter (7) is provided between the gate electrode of said first FET (1) and the local oscillation signal input terminal (8) to prevent the IF signal mixed down by the mixer circuit from leaking to the local oscillation signal input terminal (8).

Fig. I

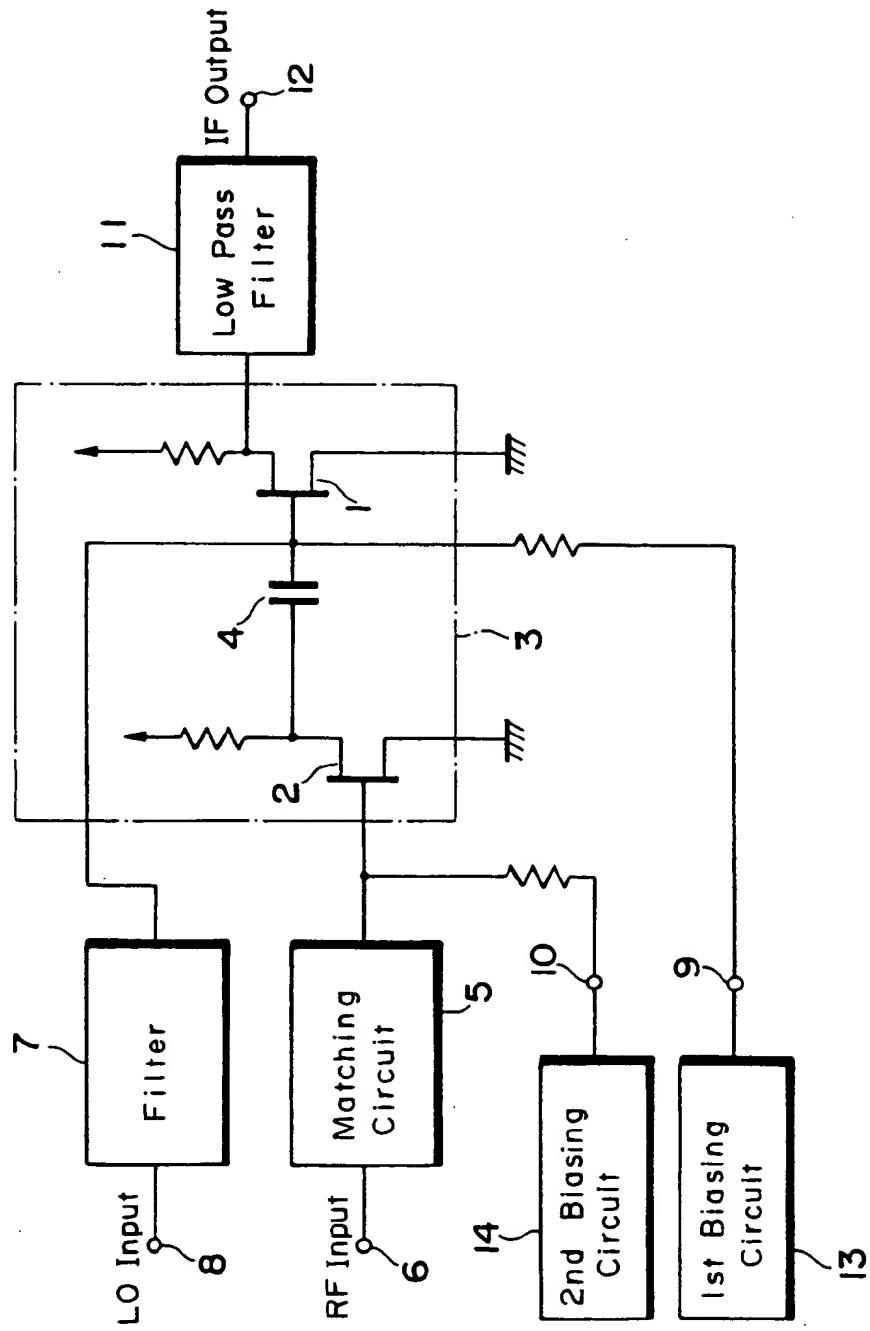


Fig. 2

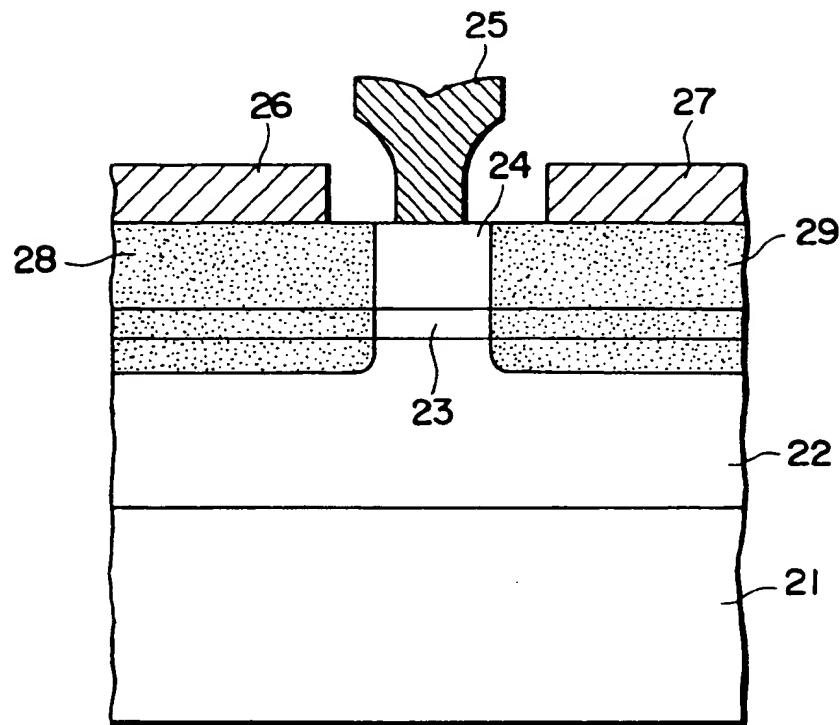
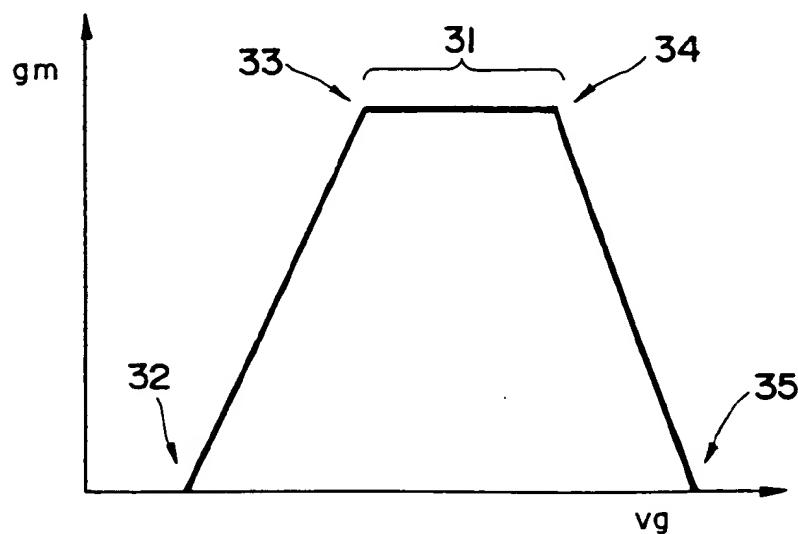


Fig. 3





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 93 10 3578

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
A	FR-A-2 587 154 (ENERTEC.) * page 10, line 27 - page 11, line 22; claim 1; figure 2 * ---	1	H03D7/12
A	US-A-5 091 759 (HUNG-DAH SHIH ET. AL.) * column 2, line 56 - column 3, line 7; figure 1 * * column 3, line 54 - column 4, line 31; claims 1,2,4 *	1	
A	QST AMATEUR RADIO vol. 52, no. 12, 1 December 1968, NEWINGTON, US pages 18 - 19 C. BUTTSCHARDT 'A CONVERTER FOR VHF FM' * page 18, column 1, line 8 - column 2, line 9; figure 1 *	1	
A	QST AMATEUR RADIO vol. 51, no. 9, 1 September 1967, NEWINGTON, US pages 11 - 12 D. DEMAW 'A LOW-NOISE CONVERTER FOR 144 MC.' * figure 1 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03D
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	21 JUNE 1993	BUTLER N.A.	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : member of the same patent family, corresponding document	
X : particularly relevant if taken alone	Y : particularly relevant if combined with another document of the same category		
A : technological background	O : non-written disclosure		
P : intermediate document			

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.